Design and Performance Analysis of Sequential Circuit Using Clocking Techniques: Survey

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Abstract – We present a new paradigm for clock distribution that uses current, rather than voltage, to distribute a global clock signal with limited power consumption. While current-mode (CM) signalling has been used in one-to-one signals, this is the main usage in a one-to-many clock distribution network. To accomplish this, we create a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) by 45 nm CMOS technology. When the CMPFFE is combined with a CM transmitter, the first CM clock distribution network exhibits 62% lower average power compared to traditional voltage mode clocks.

Index Terms – Clock distribution network, Crosstalk, Current-mode, Flip-flop, Low-power.

1. INTRODUCTION

In the past, the main concerns of VLSI designers were area, cost, performance and reliability. In circuit design power dissipation is important concern. The latest advancement in computing technology has started up a goal for high performance with low power consumption for VLSI designing engineers. Flip flops are important state holding and timing elements in digital circuits. The performance of D flip flop is more important to conclude the performance of the whole circuit. With increasing use of mobile devices, consumer electronics market need a stringent constraint on reducing power consumption. Designers are striving for small area, low power and higher speed by increasing demand of portable devices. Several researchers have worked on flip flops but they concentrates on one or few types of flip flops and applications.

In[1], Atul Katoch, Harry Veendrick and Evert Seevinck,As the technology scales, the global wire delay becomes a main bottleneck in realizing high performance SOC's. Apart from the technological efforts being made to overcome this issue, it is necessary to develop advanced circuit design techniques. This paper presents three current-mod circuits for high-speed signal propagation crosswise long on-chip busses. Theoretical search has shown that a factor of three can be gained in reproduction delay when current-mode (CM) signaling is used in comparison to voltage-mode (VM)[3]. In this paper we show that the delay is shortened by more than a factor of 2 in current mode signaling by using the circuit facility we propose in comparison to voltage-mode signaling in 0.13µm CMOS technology. This is without any significant power cost. Further gains in speed are production at very high power consumption. The power dissipation on on-chip busses is a capable function of bus layout and data rate. We identified data amount for which the proposed current mode signaling circuits come much power efficient compared to voltage mode signaling circuits.

In[2],Magdy A. El-Moursy and Eby G. Friedman. Exponentially tapered interconnect can reduce the dynamic power dissipation of clock distribution networks. A criterion for sizing H-tree clock networks is proposed. The technique reduces the power dissipated by an example clock network by up to__ while preserving the signal transition times and propagation delays. Furthermore, the inductive behaviour of the interconnects is reduced, decreasing the inductive noise. Exponentially tapered interconnects reduce by approximately the difference between the overshoots in the signal at the input of a tree as compared to a uniform tree with the same area overhead.

In[3] Ravi Teja Kumar1, K. Ramesh2 **.** Memory elements play a vital role on Digital World. In memory devices the most important factor is power consumption. Because the power consumption of the memory device increases means, the device reliability and life time is reduced. The basic memory elements of designer considerations are Latch and Flip-flop. In this paper we design SRAM using arrays of flip-flops and we analyze the design of Single-bit Flip-flop (SBFF i.e., 1bit) and made performance comparison over the Multi-bit Flip-flop (MBFF i.e., 2bit, 4bit, 8bit, 16bit, and 32bit). While designing the memory by using SBFF means it consumes more power. To get maximum reduction in power an algorithm has been proposed in which Single-bit flip flops are replaced with maximum possible Multi-bit Flip-flop without affecting the performance of the original circuit. This paper analyzes the timing performance of both SBFF and MBFF in Xilinx Virtex-5 family (XC5VLX50). These results in favour of Multi-Bit Flip-flop as reduction of power and area.

In[4],I Divona Priscilla and R Aun Prasath.In Integrated Circuit industry power has become a major contribution. The main attribute is the clock power in circuits of VLSI. In today's VLSI design scenario, power utilization by clocking takes up a vital role especially in design that uses deeply scaled CMOS technology. Proficient power utilization tends to be an important constraint in modern IC design. The underneath idea of multi bit flip flop is to reduce the inverter number by sharing among flip flop. Indulging multi bit flip flop in synchronous design is becoming a considerable method for reducing clock power. The single bit flip flop cells uses a mutual number of inverter that possess high driving capability to drive over clock signal. Grouping of such cells to form multi bi flip flop can spare drive strength, dynamic power and area of common inverter where there is no compromise among the necessary constraint among area and power. In this paper, a Hausdorff clustering algorithm is utilized to obtain nearest clustering for merging flip flops. The multi bit technique is introduced in FIR circuit to lessen power as well as area. This satisfies with the above given constraints. According to the experimental results, our algorithm significantly reduces clock power by 25.8% and it is found that total gate count is reduced from 186 to 128. The delay is curtailed upto 1.19 ns which increases the speed.

In[5], M.Ananthi, C.Sathish Kumar.In memory devices the most important factor is power consumption. Because the power consumption of the memory device increases means, the device reliability and life time is reduced. By using the array of flip-flops the SRAM is designed. The clock network of the flip-flop consumes more power. To reduce this power, the Single-Bit Flip-Flop (SBFF) is replaced by Multi-Bit Flip-Flop (MBFF). While designing the memory by using SBFF means it consumes more power. So MBFF is used to design the memory. The general type of SRAM performs a single operation (Read or Write) in each clock pulse, depending on its control signal. To overcome this limitation, QDR SRAM is designed. It has many real time applications like high speed communications, military applications, etc. In here QDR SRAM is designed by using MBFF.

In[6], Kalarikkal Absel, Lijo Manuel, and R. K. Kavitha. In this paper, we introduce a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF. The proposed designs eliminate the large capacitance present in the precharge node of several state-of-the-art designs by following a split dynamic node structure to separately drive the output pull-up and pulldown transistors. The DDFF offers a power reduction of up to 37% and 30% compared to the conventional flip-flops at 25% and 50% data activities, respectively. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons made in a 90 nm UMC process show a power reduction of 27% compared to the Semidynamic flip-flop, with no degradation in speed performance. The leakage power and process-voltage-temperature variations of various designs are studied in detail and are compared with the proposed designs. Also, DDFF and DDFF-ELM are compared with other state-of-the-art designs by implementing a 4-b synchronous counter and a 4-b Johnson up-down counter. The performance improvements indicate that the proposed designs are well suited for modern high-performance designs where power dissipation and latching overhead are of major concern.

In[7], Evert Seevinck, Petrus J. van Beers, and Hans Ontrop. The speed of VLSI chips is increasingly limited by signal delay in long interconnect lines. A simple analysis shows that mJor speed improvements are possible when using current-mode rather than conventional voltage-mode signal transporting techniques. The key to this approach is the use of low-resistance current-signal circuits to drastically reduce the impedance level and the voltage swings on long interconnect lines.As an example, a simple four-transistor current-sense amplifier forfast CMOS S W ' s is proposed. The circuit presents a virtual short circuit to the bit lines, thus reducing the sensing delay, and rendering itpractically insensitive to the bit-line capacitance. In addition, the virtual short circuit ensures equal bit-line voltages, thus eliminating the need for bit-line equalization during a read access.

In[8], Sudha Kousalya1 & G.V.R.Sagar2. Low power has emerged as a principal theme in today's electronics industry. Over the past decade, the power consumption of VLSI chips has constantly been increasing. In Integrated Circuit, there is a need of data to communicate among logic gates using flip-flop (FF). In a FF, a huge portion of the on-chip power is consumed by clock systems, which consists of timing elements such as FFs, latches and clock distribution network. These components consume 30% to 60% of the total power in a system. So to reduce Power dissipation, various conventional methods are implemented using TSPC but there is a discharging path problem. To reduce long discharging, various methods have been implemented. The existing signal feed through scheme is implemented to reduce discharging problem, but pit-falls to a new pass transistor because of its direct charging and discharging. Another drawback is more number of transistors used and power consumption is also high. The proposed Low Power Pulse Triggered Flip-Flop Design with Conditional Pulse Enhanced Technique overcomes the long discharging path problem. This method is composed of pass transistor logic (PTL) based AND gate and an extra pass transistor used at clock system. The results shown based on post layout simulation using Tanner Software CMOS 45nm technology. The proposed method improves power consumption and delay.

In[9], Kavita Mehta, Neha Arora, and Prof.B.P.Singh. This paper enumerates low power, high speed design of D flip-flop. It presents various techniques to minimize subthershold leakage power as well as the power consumption of the CMOS

circuits. The proposed circuit in this paper shows a design for D flip flop to increase the overall speed of the system as compared to other circuits. This technique allows circuit to achieve lowest power consumption with minimum transistor count.

In[10], Hardeep Kaur, Er.Swarnjeet Singh, Sukhdeep Kaur. The field of digital electronics has been directly towards to the low power digital system. The use of very large scale integration technology in high performance computing, wireless communication, consumer electronics has been rising at a very fast rate. The challenge for VLSI technology is growing in leakage power consumption. Wide utilizations of memory storage systems in modern electronics triggers a demand for high performance and low area implementation of basic memory component and one of the most state holding element is D Flip Flop. In this paper analysis of power, delay, area and power delay product is done for D flip flop using different technologies like static CMOS, C2MOS, POWER PC, GDI MUX, TSPC, etc. Low power Flip flops are useful for the design of low power digital system. The analysis and the comparison is done using TANNER EDA Tool at 130nm Technology.

2. CONCLUSION

The design has been implemented with a fresh technique at the pulse generator (clock system) i.e., PTL based AND with two transistors placed as parallel to speed up the clock pulse and reduces the number of transistors in discharging path, hence area and power are also decrease. This flip flop design reduces the discharging path problem. In this paper we presented various current-mode circuit techniques for on-chip signaling which show a speed gain of more than a factor of two in comparison to voltage mode circuits. This improvement is without much power penalty specially, at high data rates. At lower data rates (<350Mb/s) the static current consumption dominates the total power consumption, which is absent in the voltage-mode schemes. Measurement results of different voltage and current-mode signaling schemes verify the simulated values for speed. To summarize we presented three current-mode circuits; single-ended, differential and pulse based current-mode circuits. First two circuits are very suitable in applications where high data activity is expected. The third circuit has a lower static current consumption still offering 2 times speed advantage and is suitable for low latency applications where low data activity is expected.

REFERENCES

[1] Atul Katoch, Harry Veendrick and Evert Seevinck. “High Speed Current-mode Signaling Circuits for On-Chip Interconnects”, ieee 2005.

[2] Magdy A. El-Moursy and Eby G. Friedman. “Exponentially Tapered H-Tree Clock Distribution Networks”,ieee 2004.

[3] K. Ravi Teja Kumar,K. Ramesh. “Implementation of SRAM Array by Using Multibit Flip-Flop” international journal of research in computer applications and robotics,Vol.3 Issue.4,Pg: 74-79 April 2015.

[4] I Divona Priscilla, R Aun Prasath. “Design of Multi Bit Flip Flop in FIR Application Using Clustering Algorithm” International Journal of Computational Intelligence and Informatics, Vol. 3: No. 4, January - March 2014.

[5] M.Ananthi, C.Sathish Kumar, “QDR SRAM Design Using Multi-bit Flip-Flop” International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 4, Issue 3, March 2015.

[6] Kalarikkal Absel, Lijo Manuel, and R. K. Kavitha, “Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic” ieee transactions on very large scale integration (VLSI) systems, Vol. 21, No. 9, September 2013.

[7] Evert Seevinck, Petrus J. van Beers and Hans Ontrop ,“Current-Mode Techniques for High-speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAM’s” ieee journal of solid-state circuits, Vol. 26, No. 4, April 1991.

[8] Sudha Kousalya & G.V.R.Sagar “Low-Power Pulse Triggered Flip Flip-Flop Design with Conditional Pulse Enhancement Method” IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Volume 5, Issue 4, Ver. I (Jul - Aug. 2015), PP 49-56.

[9] Kavita Mehta, Neha Arora, and Prof.B.P.Singh. “Low Power Efficient D Flip Flop Circuit” International Symposium on Devices MEMS, Intelligent Systems & Communication (ISDMISC) ,2011.

[10] Hardeep Kaur, Er.Swarnjeet Singh, Sukhdeep Kaur.“Design and Analysis of D Flip Flop Using Different Technologies” International Journal of Innovative Research in Computer and Communication Engineering, Vol. 3, Issue 7, July 2015.